UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/041,071	12/28/2001	Andrew F. Glew	42390.P13769	5239

7590 10/06/2005

John P. Ward, Esq.
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, CA 90025-1026

EXAMINER	
TESLOVICH, TAMARA	
ART UNIT	PAPER NUMBER
2137	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/041,071	GLEW ET AL.	
	Examiner	Art Unit	
	Tamara Teslovich	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____. 2002: 10/10, 11/12, 11/19, 11/27
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the application filed December 28, 2001.

Claims 1-34 are pending and considered below.

Specification

The disclosure is objected to because of the following informalities: Paragraph 1 of the Applicant's Specification refers to two copending applications but fails to provide the Application numbers in addition to quoting an erroneous filing date for the two. The United States Patent Application Nos. 10/039,961 and 10/039,595, respectively entitled "Processor Supporting Execution of an Authenticated Code Instruction" and "Authenticated Code Module" were both filed December 31, 2001. Appropriate correction is required.

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not

obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:

(1) if a machine or apparatus, its organization and operation;

(2) if an article, its method of making;

(3) if a chemical compound, its identity and use;

(4) if a mixture, its ingredients;

(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

The abstract of the disclosure is objected to because it fails to sufficiently disclose the present invention. Correction is required. See MPEP § 608.01(b).

Claim Objections

Applicant is advised that should claim 32 be found allowable, claim 33 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim 12 objected to because of the following informalities: The Examiner believes that the phrase 'the key form a token' in claim 12, should instead read 'the key from a token' and for purposes of examination in the immediate action, will treat it as such. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3-5 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "like a" in claim 3 is a relative term which renders the claim indefinite. The term "like a" is not defined by the claim, the specification does not

provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Applicant's use of the phrase "like a" parallels the use of the phrase "similar" and is objectionable for the same reasons. The term "similar" in the preamble of a claim that was directed to a nozzle "for high-pressure cleaning units or similar apparatus" was held to be indefinite since it was not clear what applicant intended to cover by the recitation "similar" apparatus. Ex parte Kristensen, 10 USPQ2d 1701 (Bd. Pat. App. & Inter. 1989). See MPEP 2173.05(b), part C.

A claim in a design patent application which read: "The ornamental design for a feed bunk or similar structure as shown and described." was held to be indefinite because it was unclear from the specification what applicant intended to cover by the recitation of "similar structure." Ex parte Pappas, 23 USPQ2d 1636 (Bd. Pat. App. & Inter. 1992).

Claim 3 also recites the limitation "the processor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claims 4 and 5 depend on claim 3 and are rejected accordingly.

Claim 10 also recites the limitation "the processor" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 6-9, and 11-34 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,401,208 B2 by Davis et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Davis discloses a method comprising transferring an authenticated code module to a private memory and executing the authenticated code module stored in the private memory in response to determining that the authenticated code module stored in the private memory is authentic (col.5 lines 9-16 and 55-67; col.6 lines 1-13).

Regarding claim 2, Davis discloses transferring a number of bytes specified by an operand from a memory (col.5 lines 17-65).

Regarding claim 6, Davis discloses determining whether the authenticated code is authentic based upon a digital signature of the authenticated code module (col.5 line 66 thru col.6 line13).

Regarding claim 7, Davis discloses obtaining a first value from the authenticated code module stored in the private memory; computing a second value from the authenticated code module; and determining that the authenticated code module is authentic in response to the first value and the second value having a predetermined relationship (col.5 line 65 thru col.6 line 13).

Regarding claim 8, Davis discloses retrieving a key decrypting a digital signature of the authenticated code module with the key to obtain a first value, hashing the authenticated code module to obtain a second value; and executing the authenticated code module in response to the first value and the second value having a predetermined relationship (col.5 line 65 thru col.6 line 19).

Regarding claim 9, Davis discloses wherein decrypting comprises using the key to RSA-decrypt the digital signature, and hashing comprises apply a SHA-I hash to the authenticated code module to obtain the second value (col.3 lines 37-40; col.4 lines 29-40).

Regarding claim 10, Davis discloses retrieving the key from the processor (col.5 line 65 thru col.6 line 13).

Regarding claim 11, Davis discloses retrieving the key from a chipset (col.4 lines 15-27).

Regarding claim 12, Davis discloses retrieving the key from a token (col.4 lines 21-59).

Regarding claim 13, Davis discloses receiving the authenticated code module from a machine readable medium (col.4 lines 41-59).

Regarding claim 14, Davis discloses A computing device, comprising a chipset, a memory coupled to the chipset, a machine readable medium interface to receive an authenticated code module from a machine readable medium, a private memory coupled to the chipset, and a processor to transfer the authenticated code module from the machine readable medium interface to the private memory and to authenticate the authenticated code module stored in the private memory (col.3 lines 6-55).

Regarding claim 15, Davis discloses a memory controller coupled to the memory and a separate private memory controller coupled to the private memory (col.3 lines 14-24; col.4 lines 1-28).

Regarding claim 16, Davis discloses wherein the chipset comprises a key, and the processor authenticates the authenticated code module stored in the private memory based upon the key of the chipset (col.4 lines 15-27).

Regarding claim 17, Davis discloses wherein the processor comprises a key and authenticates the authenticated code module stored in the private memory based upon the key of the processor (col.4 lines 15-27).

Regarding claim 18, Davis discloses a token coupled to the chipset, the token comprising a key, wherein the processor authenticates the authenticated code module stored in the private memory based upon the key of the token (col.4 lines 21-59).

Regarding claim 19, Davis discloses A computing device, comprising a chipset, a machine readable medium interface to receive an authenticated code module from a machine readable medium, and a processor coupled to the chipset via a processor bus, the processor to transfer the authenticated code module from the machine readable medium interface to a private memory of the processor and to authenticate the authenticated code module stored in the private memory (col.3 lines 6-55).

Regarding claim 20, Davis discloses wherein the private memory is coupled to the processor via a dedicated bus (col.3 lines 14-25; col.4 lines 1-14).

Regarding claim 21, Davis discloses wherein the private memory is internal to the processor (col.4 lines 21-59).

Regarding claim 22, Davis discloses wherein the private memory comprises internal cache memory of the processor (col.4 lines 29-59).

Regarding claim 23, Davis discloses other processors coupled to the chipset via the processor bus, wherein the processor further locks the processor bus to prevent the other processors from altering the authenticated code module (col.4 lines 1-27).

Regarding claim 24, Davis discloses a computing device, comprising a memory, a chipset comprising a memory control that defines a portion of the

memory as private memory, a machine readable medium to receive an authenticated code module from a machine readable medium, and a processor to transfer the authenticated code module from the machine readable medium interface to the private memory and to authenticate the authenticated code module stored in the private memory (col.3 lines 6-55).

Regarding claim 25, Davis discloses wherein the chipset comprises a memory controller coupled to the memory and a separate private memory controller coupled to the private memory (col.3 lines 14-24; col.4 lines 1-28).

Regarding claim 26, Davis discloses wherein the chipset comprises a key, and the processor authenticates the authenticated code module stored in the private memory based upon the key of the chipset (col.4 lines 15-27).

Regarding claim 27, Davis discloses wherein the processor comprises a key and authenticates the authenticated code module stored in the private memory based upon the key of the processor (col.4 lines 15-27).

Regarding claim 28, Davis discloses a token comprising a key, wherein the processor authenticates the authenticated code module stored in the private memory based upon the key of the token (col.4 lines 21-59).

Regarding claim 29, Davis discloses a machine-readable medium comprising one or more instructions that in response to being executed result in a computing device transferring an authenticated code module to a private memory associated with a processor, and executing the authenticated code module stored in the private memory in response to determining that the

authenticated code module stored in the private memory is authentic (col.5 lines 9-16 and 55-67; col.6 lines 1-13).

Regarding claim 30, Davis discloses wherein the one or more instructions in response to being executed result in the computing device determining whether the authenticated code is authentic based upon a digital signature of the authenticated code module (col.5 line 66 thru col.6 line13).

Regarding claim 31, Davis discloses wherein the one or more instructions in response to being executed result in the computing device obtaining a first value from the authenticated code module stored in the private, computing a second value from the authenticated code module, and determining that the authenticated code module is authentic in response to the first value and the second value having a predetermined relationship (col.5 line 65 thru col.6 line 13).

Regarding claim 32, Davis discloses wherein the one or more instructions in response to being executed result in the computing device retrieving an asymmetric key, decrypting a digital signature of the authenticated code module with the asymmetric key to obtain a first value, hashing the authenticated code module to obtain a second value, and initiating execution of the authenticated code module in response to the first value and the second value having a predetermined relationship (col.5 line 65 thru col.6 line 19).

Regarding claim 33, Davis discloses wherein the one or more instructions comprises a launch instruction that in response to being executed results in the computing device retrieving an asymmetric key, decrypting a digital signature of

the authenticated code module with the asymmetric key to obtain a first value, hashing the authenticated code module to obtain a second value, and initiating execution of the authenticated code module in response to the first value and the second value having a predetermined relationship (col.5 line 65 thru col.6 line 19).

Regarding claim 34, Davis discloses wherein the one or more instructions in response to being executed result in the computing device receiving the authenticated code module via a machine-readable medium interface (col.3 lines 37-40; col.4 lines 29-40).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 5,732,238 by Andras Sarkozy has been included by the Examiner as evidence of the inherent use of non-volatile caches within systems for providing data integrity such as that of the present invention.

The Examiner would also like to bring the Applicant's attention the following list of US Patents which although not relied upon in the present Office Action, can be relied upon in subsequent actions if needed to fully disclose the present invention:

US Patent No. 6,633,981 B1 by Davis

US Patent No. 5,844,986 by Davis

US Patent No. 6,571,335 B1 by O'Donnell et al.

US Patent No. 5,953,502 by Helbig

US Patent No. 6,212,635 B1 by Reardon

US Patent No. 6,175,924 B1 by Arnold

US Patent No. 3,996,449 by Attanasio

US Patent No. 6,651,171 by England et al.

US Patent No. 5,737,569 by Nadir et al.

US Patent No. 5,469,557 by Salt et al.

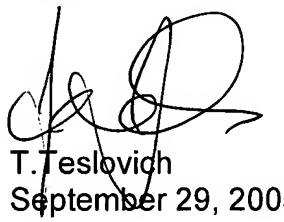
US Patent No. 5,574,936 by Ryba et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tamara Teslovich whose telephone number is (571) 272-4241. The examiner can normally be reached on Mon-Fri 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571) 272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

MATTHEW SMITHERS
PRIMARY EXAMINER
Art Unit 2137

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



T.Teslovich
September 29, 2005